



**1 General Description**

The NJ2020 is a low power baseband processor for indoor assisted Global Positioning System (A-GPS) and enhanced performance stand alone GPS applications. With the companion NJ1006A GPS RF front end and the NS2020 navigation software, all components are provided to smoothly integrate A-GPS into an existing host system and exceed the 3GPP 25.171 and TIA-916 performance requirements. This allows mobile phone emergency applications (E911, E112) and offers in addition the performance and flexibility suitable for development of emerging Location Based Services (LBS) with indoor requirements.

Based on a hosted architecture, the NJ2020 reuses the processor, memory, interfaces and system support functions of the target system achieving the lowest possible Bill of Material (BOM) and board real-estate. The NS2020 navigation software places no real time constraints on the host processor, occupies a minimal memory footprint and requires between 5 to 10 MIPS, thus making the NJ2020 a very low impact and low risk solution for adding A-GPS location capabilities to a system.

The NJ2020 has been developed using Nemerix methodologies for ultra low power consumption. The very short fix time using the NJ2020 powerful correlation processor, paired with the NJ1006A low power, low noise GPS front end provides minimal energy to fix but also continued low power consumption during harsh indoor navigation conditions. A series of power management modes are in place to insure low power operation for a variety of conditions and a multitude of system platforms.

All three A-GPS modes are supported: Mobile Station (MS) based, MS assisted and stand alone. The tracking sensitivity is as low as -159dBm, Time To First Fix (TTFF) is less than 2s outdoor and 7s indoor while accuracy (RMS)

goes from 5m outdoor to 35m indoor. A powerful correlation engine supports asynchronous and synchronous networks equally well.

The system accepts a large variety of clocking sources and frequency plans. A UART, or SPI or I<sup>2</sup>C can be used to interface the NJ2020 to the host system. The navigation software embedded in the host processor offers an Application Programming Interface (API) to implement assistance protocols at the user plane (e.g. SUPL) or the control plane (RRLP & RRC) level. The same API can be used to develop LBS services directly interacting with the A-GPS navigation engine.

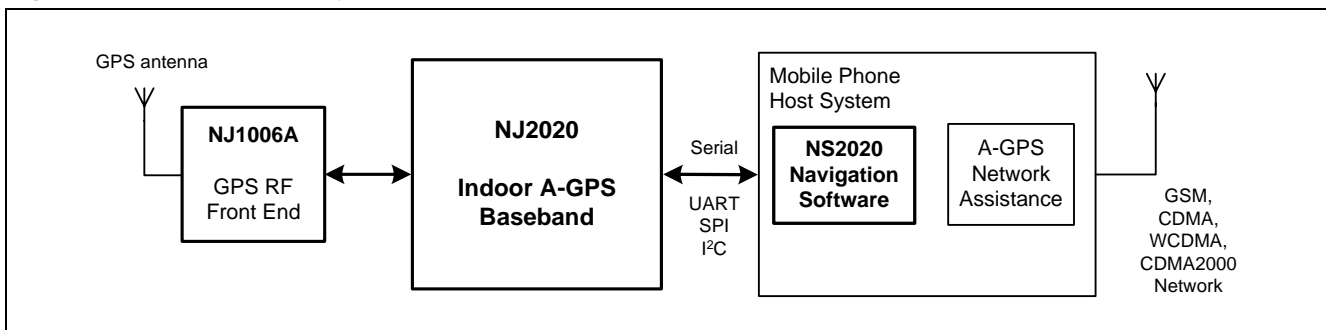
**1.1 Features and benefits**

- Hosted, A-GPS for lowest cost and smallest size
- Low system impact and risk, no real time constraints
- Exceeds 3GPP and TIA performance requirements
- Ultra low power consumption
- UART, SPI slave or I<sup>2</sup>C slave host interface
- MS-Based, MS-Assisted and stand alone operation
- Asynchronous (e.g. GSM/WCDMA) and synchronous (e.g. IS-95/IS-2000) networks supported
- SW API for a tighter integration or serial interface
- Targeting fix-on-request and continuous navigation
- Packaging: 6x6mm, 0.5mm pitch, 81 balls (μBGA)–Lead-free, RoHS compliant

**1.2 Applications**

- Mobile phones and smart phones
- PDAs and Portable Media Players (PMP)
- Asset tracking, fleet management
- Emergency applications (E911, E112)

**Figure 1: A-GPS cell phone system based on NJ2020 and NJ1006A**



**NO PARTS OF THIS PUBLICATION MAY BE REPRODUCED, PHOTOCOPIED, STORED ON A RETRIEVAL SYSTEM, OR TRANSMITTED WITHOUT THE EXPRESS PRIOR WRITTEN PERMISSION OF NEMERIX SA**

© 2005 Nemerix SA. All rights Reserved. Nemerix SA assumes no responsibility for this product's use, nor for any infringement of patents or other rights from third parties which may result from its use. No license is implied under any patent or patent right by Nemerix SA, CH-6928 Manno, Switzerland

**2 Table of contents**

**1 General Description..... 1**

1.1 Features and benefits..... 1

1.2 Applications..... 1

**2 Table of contents ..... 2**

**3 Absolute Maximum Ratings..... 3**

**4 Electrical Characteristics ..... 3**

4.1 Power Supply ..... 3

4.2 AC Electrical Characteristics ..... 3

4.3 Digital Interfaces..... 3

**5 GPS Performance ..... 4**

5.1 Specifications ..... 4

**6 Pinout..... 5**

6.1 Power Supply and Reset..... 5

6.2 Digital Interfaces..... 5

6.3 GPS RF interface ..... 6

6.4 Analog..... 6

6.5 Debug Interfaces ..... 6

6.6 Not Connected ..... 6

**7 Architecture..... 7**

7.1 Functional partitioning ..... 7

7.2 Block diagram..... 8

7.2.1 RF interface ..... 8

7.2.2 GPS correlation engine ..... 8

7.2.3 DSP subsystem ..... 8

7.2.4 Split power supply: CC and SP domains ..... 9

7.2.5 System Boot Options ..... 9

7.2.6 Host interfaces..... 9

7.2.7 Other peripherals..... 9

7.2.8 Debug/Emulation ..... 9

7.2.9 Analog Functions..... 9

**8 Interfacing ..... 10**

**9 Clocking..... 12**

9.1 Reference Clock..... 12

9.2 Auxiliary Oscillator..... 12

**10 Power Supplies ..... 13**

**11 Application Examples..... 14**

11.1 Cell phone host ..... 14

11.2 PDA Host..... 15

**12 Packaging..... 16**

**13 PCB Layout Recommendations..... 16**

**14 Mounting Recommendations..... 17**

**15 Physical Dimensions ..... 19**

### 3 Absolute Maximum Ratings

Max padding supply voltage..... 4V	Continuous power dissipation .....300mW
Max core supply voltage..... 1.5V	Operating temperature .....-40 to +85°C
Max. current into any pin except power supplies..... ±20mA	Junction temperature ..... 125°C
Max current into power supply..... ±50mA	Storage temperature .....-65 to +150°C
ESD Rating (HBM) ..... TBD	Lead temperature (soldering, 10s) .....250°C

Absolute maximum ratings are short term stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions is not implied. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.



**ESD sensitive device: use proper precautions when handling this device.**

### 4 Electrical Characteristics

DVDD=1.6V to 3.6V, DAVDD=1.6V to 3.6V, TVDD = 1.6V to 3.6V, LVDD\_CC = 1.2V, LVDD\_SP = 0.9V to 1.2V, T<sub>amb</sub>=-40 to +85°C, load = 10 pF, crystal oscillator active, unless otherwise noted. All voltages are referred to xVSS. Typical values are at xVDD = 1.8V, LVDD\_CC = 1.2V, LVDD\_SP = 1.2V, T<sub>amb</sub>=+27°C.

Parameter	Conditions	Min	Typ	Max	Unit	Notes
-----------	------------	-----	-----	-----	------	-------

#### 4.1 Power Supply

DVDD,DAVDD,TVDD		1.6	1.8	3.6	V	
LVDD_CC		1.08	1.2	1.32	V	1
LVDD_SP		0.9		1.32	V	2
Current on LVDD_CC	1.2V, 72 MHz		5		mA	
Current on LVDD_SP	1.2V, 72 MHz			80	mA	3

#### 4.2 AC Electrical Characteristics

Reference Frequency		8		40	MHz	4
Internal Clock Frequency	LCDD_SP 1.2V			72	MHz	5
Auxiliary Clock Frequency			32.768	2000	kHz	6

#### 4.3 Digital Interfaces

V <sub>IH</sub>		0.7 xVDD		xVDD+0.3	V	
V <sub>IL</sub>		-0.3		0.3 xVDD	V	
V <sub>OH</sub>	-50 μA	0.9 xVDD			V	
V <sub>OL</sub>	+50 μA			0.1 xVDD	V	
Output Rise Time	Cl = 15 pF			5	ns	
Output Fall Time	Cl = 15 pF			5	ns	

#### Notes :

1. An on-chip voltage regulator is available to supply this voltage if desired
2. Can be changed dynamically. On-chip programmable regulator is available
3. Worst case, maximum current during deep-indoor, full search operation.
4. 1V<sub>pp</sub> clipped sine (TCXO) or full swing CMOS levels
5. Generated by on chip PLL
6. Accepts tuning for watch Xtal or TCXO

## 5 GPS Performance

### 5.1 Specifications

Parameter	Conditions	Min	Typ	Max	Unit	Notes
Sensitivity	Acquisition			-155	dBm	
	Tracking			-159	dBm	
Accuracy	Outdoor (RMS)	5			m	
	Indoor (RMS)	35			m	
Time To First Fix (TTFF) – Hot start or Assisted <sup>(7)</sup>	0.1 ppm clock / -133 dBm signal		1.2		s	7
	0.1 ppm clock / -148 dBm signal		7		s	7
	0.1 ppm clock / -152 dBm signal		14		s	7
	0.1 ppm clock / -155 dBm signal		31		s	7

**Notes :**

7. TTFF figures are 50% probability

## 6 Pinout

### 6.1 Power Supply and Reset

Ball Nb	Signal Name	Type	Function
G9, J3	LVDD_CC	Digital power	CC core power supply
A2, A7, E9, H3, H9, J5	LVSS	Digital ground	Core ground
F3	LDEn	Digital In	Internal / external voltage regulator selector for LVDD_CC
D6, F4, F6	DVDD	Digital power	Power supply for pad ring and voltage reg.
D5, E4-7, F5	DVSS	Digital ground	Ground
A3, A8, D9, G3	LVDD_SP	Digital power	SP core power supply
J7	PRst_n	Digital In	Active low asynchronous reset
J6	WRst_n	Digital In	Active low asynchronous reset preserving CC domain
G5	ExtPowerOK	Digital In	Input from external power supply supervisor
G4	ExtPower	Digital In	External power supply indication to DSP

### 6.2 Digital Interfaces

Ball Nb	Signal Name	Type	Function
C9	GPIO0	Digital IO	Programmable IO / UART 0 CTS In
C8	GPIO1	Digital IO	Programmable IO / Jammer Input
C7	GPIO2	Digital IO	Programmable IO / Eeprom boot
B8	GPIO3	Digital IO	Programmable IO / Aux SPI CS
B7	GPIO4	Digital IO	Programmable IO / PPS Output
C6	GPIO5	Digital IO	Programmable IO / I2C Address
B6	GPIO6	Digital IO	Programmable IO / I2C Address
A6	GPIO7	Digital IO	Programmable IO
H8	SPIMemClk	Digital Out	SPIMemClk = SPI master clock out / SCLK = scope clock out
J9	SPIMemRx	Digital IO	SPIMemRx in / SBSync out = scope synch out
F7	SPIMemSel_n	Digital Out	SPI master select 0
G8	SPIMemTx	Digital Out	SPIMemTx Out / SData out = scope data out
F9	SCL	Digital Out	I2C serial clock – Open Drain out / Schmitt in
F8	SDA	Digital Out	I2C serial data – Open Drain out / Schmitt in
C5	SPIClk	Digital In	SPI slave clock
B5	SPIRx	Digital In	SPI slave input
A4	SPISel	Digital In	SPI slave select
A5	SPITx	Digital Out	SPI slave output / SFSync out
D7	Uart0Rx	Digital In	UART1 receive
D8	Uart0Tx	Digital Out	UART0Tx out / SFSync out
B9	Uart1Rx	Digital In	Debug receive
A9	Uart1Tx	Digital Out	Debug transmit
H5	Sync	Digital In	System time sync input

### 6.3 GPS RF interface

Ball Nb	Signal Name	Type	Function
E1	TVDD	Digital power	RF interface power supply
D2	AntennaOK	Digital In	Antenna status indicator
C1	GPSInA[3]	Digital In	GPS IF input signal
C3	GPSInB[3]	Digital In	GPS IF input signal
C2	GPSInA[2]	Digital In	GPS IF input signal
C4	GPSInB[2]	Digital In	GPS IF input signal
B1	GPSInA[1]	Digital In	GPS IF input signal
B3	GPSInB[1]	Digital In	GPS IF input signal
B2	GPSInA[0]	Digital In	GPS IF input signal
B4	GPSInB[0]	Digital In	GPS IF input signal
E2	M1	Digital Out	M1 = Mode 1 out for NJ1006A
E3	M2	Digital IO	M2 = Mode 2 out for NJ1006A
D3	P0	Digital Out	P0 = Power control out to Nemerix RF
D4	P1	Digital Out	P1 = Power control out to Nemerix RF
D1	RFClk	Digital IO	GPS reference clock output to RF device
A1	AGCAn	Analog	AGC Analog Output

### 6.4 Analog

Ball Nb	Signal Name	Type	Function
F2	DAVDD	Analog power	Analog power supply
G2, H2	DAVSS	Analog ground	Analog ground
H1	LDO_SP	Analog Out	Internal LDO control line for external PNP pass transistor
F1	RefOsc	Analog In	TCXO / Digital input
J2	AuxOsc0	XTAL Osc	Crystal oscillator input
J1	AuxOsc1	XTAL Osc	Crystal Oscillator output/external oscillator input below 1MHz

### 6.5 Debug Interfaces

Ball Nb	Signal Name	Type	Function
E8	ReMap	Digital In	Select remapping for debug mode
H4	Debug	Digital In	Enable debugger
H7	TDI	Digital In	JTAG / debugger interface
G6	TDO	Digital Out	JTAG / debugger interface
J8	TCK	Digital In	JTAG / debugger interface
H6	TRST_n	Digital In	Test reset input
G7	TMS	Digital In	JTAG / debugger interface

### 6.6 Not Connected

Ball Nb	Signal Name	Type	Function
G1	NC	Not Connected	To avoid ESD problem, connect to LVSS
J4	NC	Not Connected	To avoid ESD problem, connect to LVDD_CC

## 7 Architecture

### 7.1 Functional partitioning

**Figure 2: Hosted architecture functional partitioning**

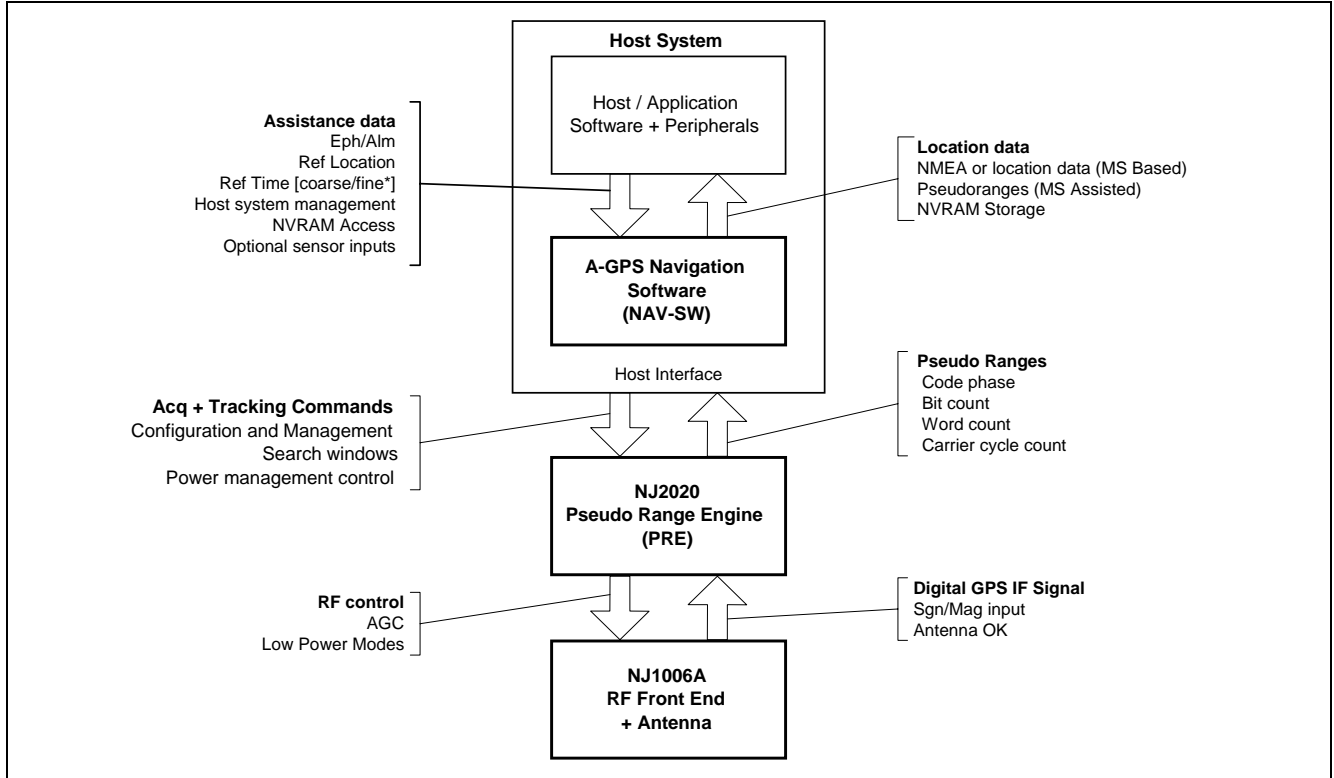


Figure 2 shows the functional partitioning of a NJ2020 based A-GPS system. The NJ2020 covers the function of a so called Pseudo Ranges Engine (PRE) where all the real time critical, computational intensive processing is executed. On the other hand, the navigation and receiver control functions are located on the navigation software (NAV-SW) module running in the host environment, where the interfacing with the user application and the network assistance can best be implemented.

Depending on the application requirements, the A-GPS receiver control functions in the NAV-SW activate the NJ2020 acquisition and/or tracking capabilities. In doing this the NAV-SW exploits any already available information in the host system such as positions and clock estimates, stored ephemeris or almanac data. This type of information can also be obtained by the NAV-SW through the assistance network. Based on the available information the NAV-SW generates a series of commands to the NJ2020 indicating how to manage the tracking and acquisition resources.

The NJ2020 implements all needed GPS signal acquisition, tracking and decoding capabilities. The commands received from the NAV-SW are executed by

configuring the acquisition and tracking resources accordingly. Once the GPS signal is acquired a series of measurements can be made on each tracked space vehicle (SV) signal. These measurements build the pseudo-range values that are given back to the NAV-SW as a result of the tracking activity.

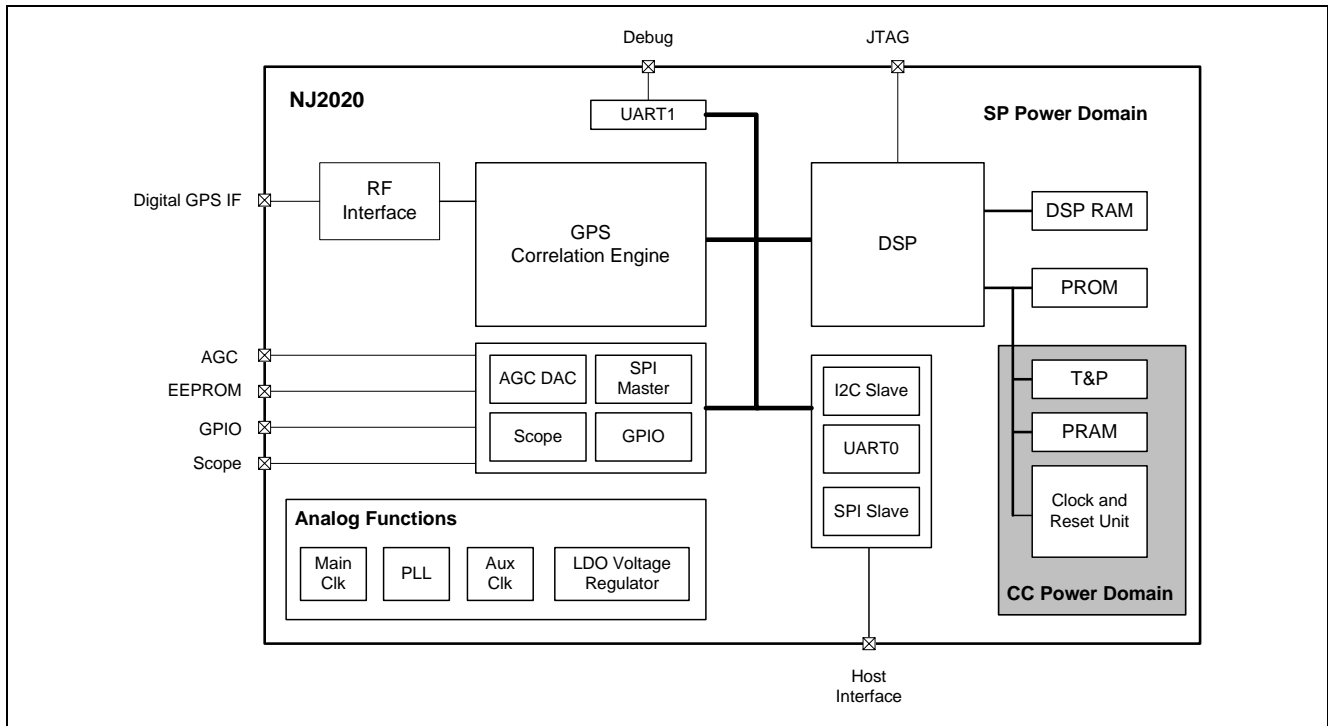
If the GPS signals are stronger than -144dBm the NJ2020 can decode the data transmitted by the GPS system and deliver ephemeris, almanac and ionospheric correction data to the NAV-SW. If the signal strength is lower, the NAV-SW will typically use pre-stored information or retrieve it from network assistance.

Based on the pseudo-range obtained and on the ephemeris, the NAV-SW is able to calculate a fix and perform navigation in case of Mobile Station (MS) based operation. For MS assisted operation pseudo-ranges values are directly forwarded (through the cell phone) to the network infrastructure requiring the data.

The NJ2020 directly controls the NJ1006A RF front end automatic gain control (AGC) and power management inputs. The NJ1006A generates the GPS IF digital signal and an Antenna-OK indicator to the NJ2020.

## 7.2 Block diagram

Figure 3: NJ2020 block diagram



The PRE functionalities described in Section 7.1 are mapped on the RF interface, the GPS correlation engine and the DSP processor. On top of that, a series of interfaces and mixed mode support functions are implemented.

### 7.2.1 RF interface

The RF interface implements the initial transformation of the digital IF signal generated by the GPS RF front end. The input IF signal, sampled at the frequency defined by the selected frequency plan, is numerically converted into the NJ2020 internal data format.

The RF interface supports single ended and I/Q signals in sign/magnitude or two's complement 2x4 bit format. The used data format and sampling frequency (between 8 MHz and 32 MHz) can be configured at system boot time. In its default configuration it directly supports the NJ1006A RF front end 2-bit sign and magnitude data format with a sampling frequency of 16.368 MHz.

### 7.2.2 GPS correlation engine

The GPS correlation engine implements the carrier frequency wipe off functions plus the coherent and incoherent integration functions in order to implement the digital processing gain necessary for indoor A-GPS applications. This flexible and powerful architecture can switch between 4 full code-space acquisition channels and up to 36 tracking channels (maximum of 14 SVs). This efficient reuse of hardware also minimizes power consumption.

Additionally, the strength of the incoming signals is dynamically determined by an Automatic Gain Control (AGC) unit so that a gain factor can be fed back to the RF front end gain control input through a dedicated interface (see 7.2.7).

### 7.2.3 DSP subsystem

The DSP subsystem implements all real time critical functions related to the GPS functionality as well as various control functions. The program memory architecture is based on a combination of RAM and ROM instances with code flexibility provided by a mechanism that permits patching from the host. This allows the access to standard ROM based functionalities and library elements as well as the implementation of customer driven requirements and software modifications on the same silicon. Moreover the program RAM (PRAM) is in the CC power domain that is typically maintained during system power downs, so that any modification to original ROM based firmware are preserved and quick recovery time can be obtained, without having to re-boot the NJ2020.

The DSP subsystem implements 3 functions: the interfacing with the host NAV-SW, the receiver management and the satellite data management. In the first case it translates the high level commands coming from the NAV-SW (running on the host) into control commands to the receiver manager. At the same time, raw GPS data and status information are sent back to the host. The receiver management consists in the

configuration and use of the correlation resources based on the available aiding and time information. The third functionality is related to the demodulation of the GPS Navigation Message in situation where sufficient signal power is present. Such navigation message is then transmitted to the host.

#### **7.2.4 Split power supply: CC and SP domains**

The power supply of the NJ2020 digital core is partitioned into a Signal Processing (SP) and a Clock & Control (CC) sub-system.

The SP power domain runs at different clock frequencies depending on required CPU performance and the core voltage is adjusted accordingly (between 0.9 V to 1.2V). For the implementation of power management modes, the SP power supply can be removed.

The CC power domain has a fixed voltage of 1.2V and it is typically maintained in power down modes. The DSP program RAM (PRAM), the clocks configuration circuits and the trap and patch unit (T&P) are located in this power supply domain because they store all the information that must be maintained to allow quick recovery from power saving modes.

#### **7.2.5 System Boot Options**

Typically the NJ2020 can boot directly from the DSP ROM. However the use of the NJ2020 in the target system typically requires some customization. For instance there may be the need to modify the frequency plan, the host interface speed or the use of the GPIO interface. As a consequence a mechanism is provided to overwrite these settings or to expand the standard SW functionality by booting the system from a) the host through the used interface or b) an external EEPROM through a dedicated SPI master interface.

#### **7.2.6 Host interfaces**

##### **UART**

The host interface UART (UART0) has a 32 bytes transmit/receive FIFO and has a programmable baud rate from 9600 to 115200 bauds. Dedicated UART0\_Tx and UART0\_Rx pins are available, while a CTS signal is multiplexed with GPIO[0] pin.

##### **SPI Slave**

The SPI slave device provides a single slave interface through which the NJ2020 can communicate with the host processor.

Clocking for the data transfer is provided from a device pin at a frequency of up to 1MHz which can be asynchronous to the system clock. Data are valid on the rising edge of this clock. Output data from the block is resynchronized to the falling edge of the SPI clock.

The SPI slave implements a 32 bytes transmit/receive FIFO's with thresholds for interrupt generation programmable to allow  $\frac{1}{4}$  and  $\frac{1}{2}$  full levels for the receive FIFO, and  $\frac{1}{4}$  and  $\frac{1}{2}$  empty levels for the transmit FIFO.

##### **I2C**

The I2C controller operates at rates up to 400 Kbits/sec, supports 7 bit addressing mode only and implements the Slave Receiver mode and Slave Transmitter mode according to the I2C specification. The I2C controller implements a 32 Bytes transmit and receive FIFO. Only 3.6V or lower level signals are supported.

#### **7.2.7 Other peripherals**

##### **Serial EEPROM**

A dedicated SPI master interface can be used to boot the system from an external EEPROM. Once the boot process is finished the EEPROM power supply is switched off.

##### **Analog and Digital AGC**

The internal AGC value generated by the correlation engine is made available to the RF front end as an analog voltage through a D/A converter. The digital AGC value can also be sent through the SPI master interface for RF front ends that support such interface.

##### **GPIO**

A general purpose Input/Output (GPIO) port with 8 signals is available.

#### **7.2.8 Debug/Emulation**

##### **Debug UART**

A dedicated UART (UART1) is available in order to display real time debug information at run time. This gives a real time insight of the GPS receiver status.

##### **JTAG**

A standard JTAG interface can be used for software development and debugging on the DSP, but also for in system connectivity tests on the PCB (boundary scan).

##### **Scope**

A scope interface serially outputs the correlation results to an external DAC so that the correlation efficiency can be monitored in real time (correlation taps on the X-axis, correlation value on Y-axis). This function allows real time identification of bursty jammers in hostile integration environments

#### **7.2.9 Analog Functions**

An on chip PLL and auxiliary oscillator (see Section 9) and on chip voltage regulators (see Section 10) are implemented in the analog function block.

## 8 Interfacing

Figure 4: NJ2020 interfacing diagram

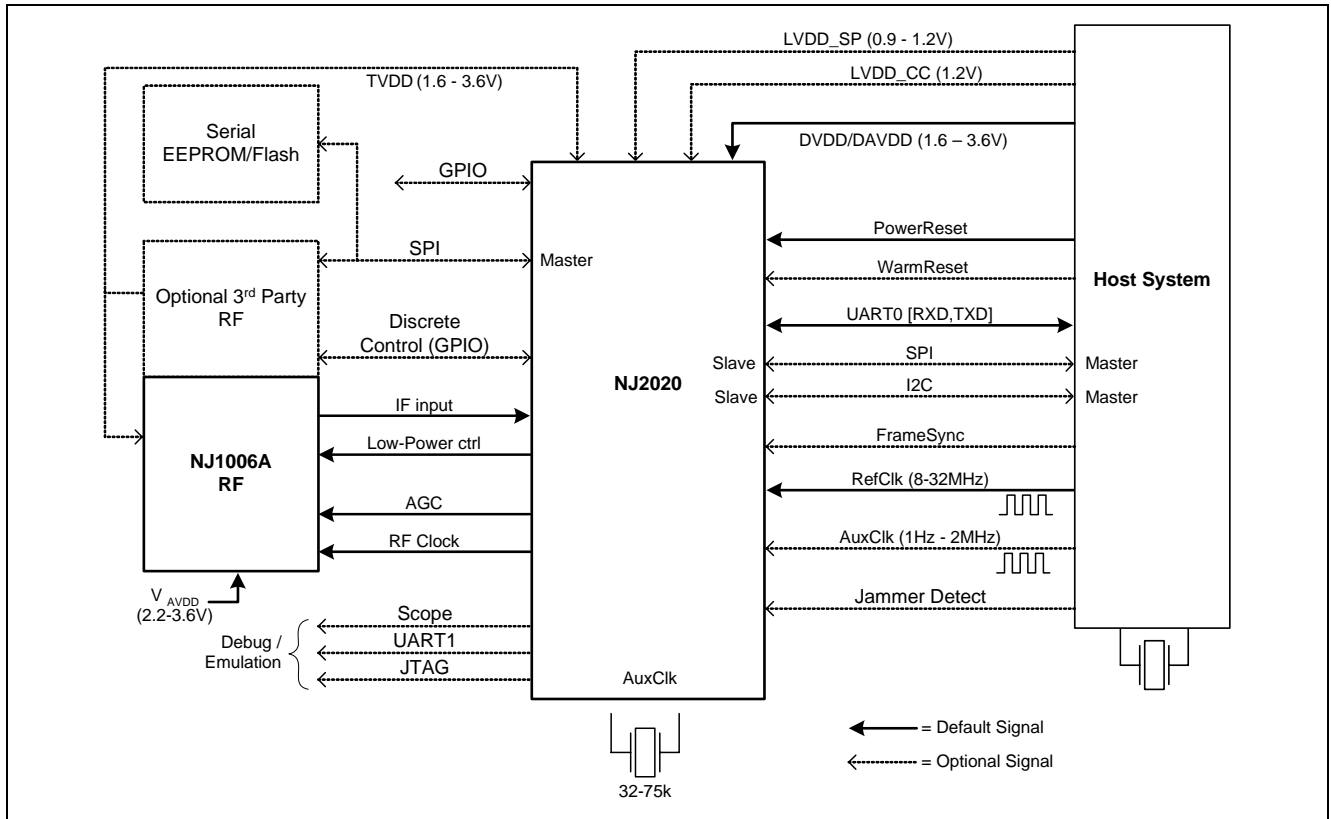


Table 1: Interfacing details

Category	Signal	Description
Supplies	DVDD	Main NJ2020 digital device supply (1.6-3.6V). Determines the voltage level of the host interface and all digital signals (excluding the ones in the TVDD domain)
	DAVDD	Main NJ2020 quiet analog power supply (1.6-3.6V).
	LVDD_CC	Optional CC digital core supply override (1.2V)
	LVDD_SP	Optional SP digital core supply override (0.9-1.2V)
	TVDD	Pad-ring supply to set IO level on RF-Interface signals. Also used for the digital interface of the NJ1006A (1.6-3.6V)
	AVDD	Dedicated, clean power supply for the NJ1006A RF section (2.2-3.6V)
Resets	PowerReset	Main reset to device – resets all logic (CC and SP) and used on device power-up by connection to DVDD. Can be controlled via a digital signal by host to reset device if lock-up suspected
	WarmReset	Resets only SP logic and used on core power-up by connection to LVDD_SP. Can be controlled via a digital signal by host to reset device if lock-up suspected

Clocking	RefClk	Main reference clock for device – can be from either a TCXO, a clock signal from the host or the NJ1006A RF (8-32MHz)
	AuxClk (osc)	Auxiliary timing reference clock for device – can be from either external digital signal or TCXO (1Hz-RefClk/2 MHz) or an integrated XTAL oscillator (32-75kHz)
Host Interface	UART	2-wire UART (with optional HW flow control) for communications between host-based NAV-SW and the PRE on NJ2020
	SPI-Slave	4-wire slave SPI controller provided on NJ2020 to connect with a SPI-Master on the host for communications between the NAV-SW and the PRE on NJ2020
	I2C Slave	2-wire I2C interface for communications between host-based NAV-SW and the PRE on NJ2020
Timing	FrameSync	A sync signal from host, usually tied to Air Interface frame timing, that can be used as a time reference by the PRE to maintain accurate time
RF	IF Input	This is a 2x4-bit digital low-IF input into the NJ2020 GPS signal processing function – for the NJ1006A only the least 2 significant bits of the IF path are required (Sgn/Mag)
	Low-Power control	P0 and P1 that control the low-power modes of the NJ1006A RF device
	AGC	Output to the NJ1006A AGC input
	RF clock	Clock input to the RF derived from RefClk (Either = RefClk, or RefClk÷2), or clock output
	Discrete Control lines	Optional discrete control lines for 3 <sup>rd</sup> party RF solutions can be provided via the GPIO pins of the NJ2020
	SPI-Master	A SPI master which can be used to control functions such as AGC on 3 <sup>rd</sup> party RF devices
Misc	GPIO	Can be used for general purpose input/output to the host device, other devices or to 3 <sup>rd</sup> party RF solutions (see Discrete Control lines above)
	JammerDetect	Intended for shared RF subsystems (eg. Antenna) to modify integration within the GPS correlation engine according to host RF activity
	SPI-Master 2 <sup>nd</sup> CS	A second CS for the SPI-Slave is provided to access optional external serial flash or EEPROM.
Debug / Emulation	UART	A second UART used for debug trace information from the embedded DSP code
	JTAG	This interface is used for embedded DSP debug as well as device boundary scan of the digital logic
	Scope Output	Serial data output to an external DAC to provide real-time debug display of correlation logic on a 'scope'

## 9 Clocking

There are two primary time references for the NJ2020 device:

- the main reference clock used for the GPS digital front-end, and as the primary time base. During all operational modes this clock is also used to drive the DSP and peripherals.
- the Auxiliary Time Reference (ATR) clock – is an optional lower-power clock used to maintain time reference during GPS idle periods and can also be used as a lower-power slower clock to the DSP in doze mode.

### 9.1 Reference Clock

Starting from the reference clock which is determined by the available sources and GPS RF constraints the PLL and a clock generation unit generate all needed internal frequencies: in particular the clock for the DSP processor, the correlation engine and the various interfaces.

The NJ2020 device accepts any input frequency in the range of 8-32 MHz. When used in conjunction with the NJ1006A RF the frequencies listed in Table 2 are supported:

**Table 2: Typical reference frequencies**

Frequency [MHz]	Standard	Frequency [MHz]	Standard
12.6	Cellular (PDC)	19.2	Cellular (CDMA), PHS
13	Cellular (GSM)	19.68	Cellular (CDMA)
14.4	Cellular (PDC, AMPS)	19.8	Cellular (CDMA)
15.36	CEPT1 (7.5X), Cellular (AMPS)	26	Cellular (Dual-mode WCDMA/GSM)
16.367/8	NJ1030 Typical GPS	30.72	Cellular (WCDMA,AMPS)

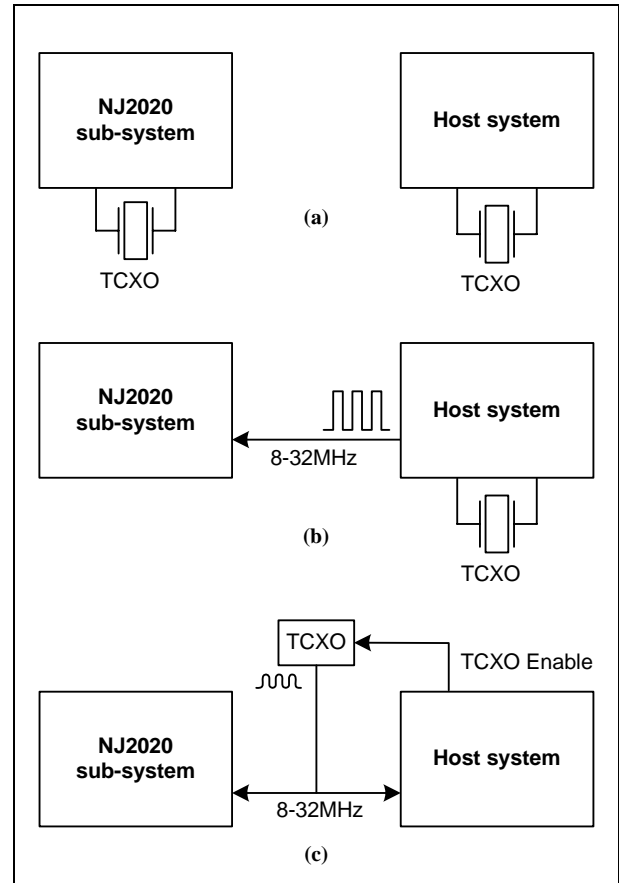
Figure 5 gives some options for obtaining the reference clock within a host system. It is assumed that the host system always maintains mastership of the reference clock and controls when it is switched on-and-off. Since the NAV-SW is running on the host and is effectively master of the GPS sub-system this should not be a problem.

Option (a) depicts the simplest arrangement, but is not very cost or power efficient. Here the NJ2020 runs off its own oscillator or external TCXO with the host system also running from its own independent oscillator.

Options (b) and (c) share an existing oscillator of the host system, with the host controlling when the oscillator is

enabled and disabled. Here software messages are used to coordinate the oscillator duty-cycling with NJ2020 power saving modes. It is left as a software integration exercise between the NAV-SW and the cell-phone power management software to arbitrate for the oscillator for GPS activity.

**Figure 5: Reference Clock Options**



### 9.2 Auxiliary Oscillator

An optional auxiliary time reference (ATR) is implemented starting from a low power 32 kHz to 75 kHz oscillator (digital clocks to up to 2MHz are also supported). The aim of this oscillator is to maintain a precise knowledge of time during system power down situations or in cases where the main oscillator is powered on/off. The ATR can then accelerate the GPS fix time, when the system is resumed.

### 10 Power Supplies

The power supply structure of the NJ2020 has been developed to cover the need of running from a minimal number of power supplies but also to re-use any already available power supply in the system. Moreover dynamic programming of the SP power supply is implemented.

The system is partitioned into the following power supply domains:

- **DVDD:** (1.6V to 3.6V) is the main digital power supply (noisy) used to a) set the voltage levels of the digital interfaces (excluding the signals in the TVDD domain) and b) to generate the CC power supplies from the on chip voltage regulator.
- **DAVDD:** (1.6V to 3.6V) is a quiet power supply for the on chip analog blocks. Typically DAVDD can directly be derived from DVDD, using a RC filter in the cases where the noise on DVDD is too high.
- **TVDD:** (1.6V to 3.6V) is a power supply that determines the voltage level of a group of digital signals interfacing to the RF front end. It may be directly connected to DVDD unless particular noise issues or low power considerations need to be addressed in interfacing the GPS RF device.
- **LVDD\_CC:** (1.2V) is the core power supply of the CC domain. It can be derived from DVDD by an on chip low drop out (LDO) voltage regulator or provided by an externally available source.
- **LVDD\_SP:** (0.9V to 1.2V): is the core power supply of the SP domain. It can typically be derived from DVDD by an on chip voltage regulator with an external PNP pass transistor, or can be provided by an external supply source. If generated on chip, its voltage level can be dynamically controlled by the NJ2020 to match the required clock speed and implement low power modes. If the source is external to the NJ2020 then its value is fixed.

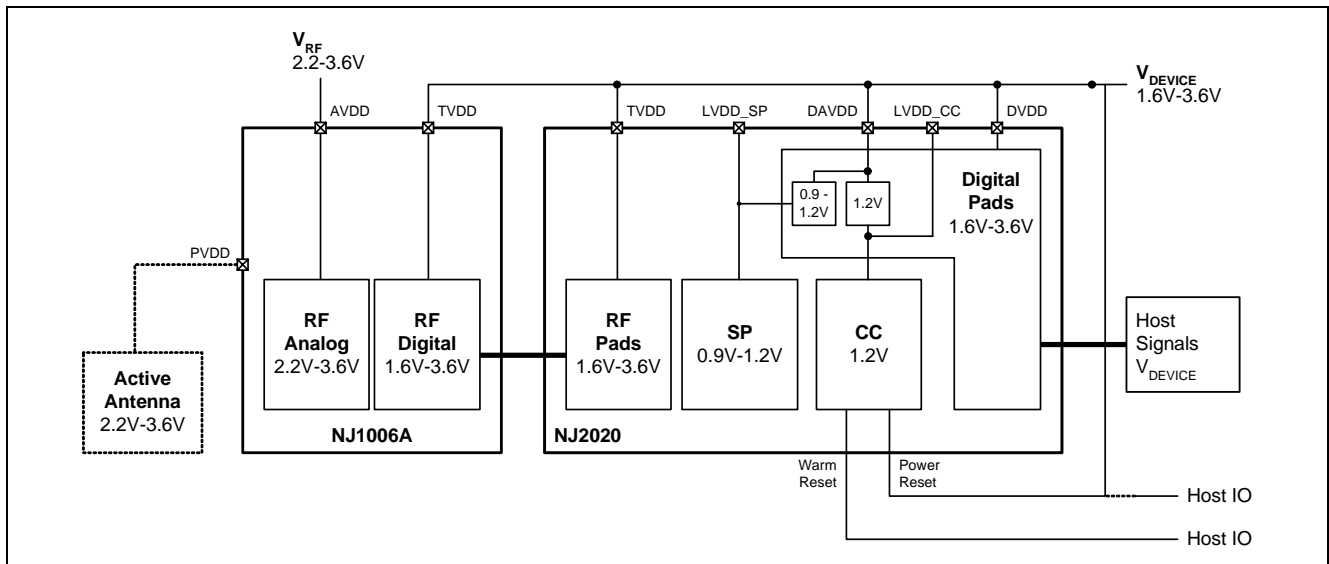
Typical power consumption measured with the first silicon version on NJ2020 running with a frequency of 16.368MHz are shown in Table 3. Fix status means that fully active software is running and able to get a valid position of the receiver. Hibernate/Sleep status means that the NJ2020 is in one of the power-save modes and ready to enter fully active mode as soon the Fix is required from Host processor. Power consumption will be further improved on the production silicon version.

**Table 3: Typical power consumption @16.368MHz**

	Voltage	Current	Status
DVDD	3.0 V	4.85 mA	Fix
		0.72 mA	Sleep
DAVDD	3.0 V	0.33 mA	Fix
		0.32 mA	Hibernate/Sleep
TVDD	3.0 V	1.27 mA	Fix
		1.27 mA	Sleep
LVDD_CC	1.2 V	3.25 mA	Fix
		0.43 mA	Hibernate/Sleep
LVDD_SP	1.2 V	53.2 mA	Fix
		5.67 mA	Sleep

Figure 6 represents a typical power supply setup where the NJ2020 is running from a single power supply source of 1.6V to 3.6V. Considering the whole GPS subsystem a second, clean power supply source of 2.2V to 3.6V is necessary for the RF stage of the NJ1006A. Typically a passive antenna is used, but the power supply for an optional active antenna can be derived from the NJ1006A directly.

**Figure 6: Typical power supply configuration with NJ2020 and NJ1006A**



### 11 Application Examples

The NJ2020 is a companion GPS Engine device, and as such can be used for a multitude of different applications with a suitable host system. Two possible host systems are considered: cell-phone and PDA.

#### 11.1 Cell phone host

Figure 7 represents the use of the NJ2020 device within a cell-phone host system. A host UART/SPI/I2C communications channel, some timing signals (optional) to provide synchronization between the cell-phone network and GPS time domains and other system support signals (such as power, clocks and resets) are required. The configuration is shown with the GPS system sharing the clock and power resources of the cell-phone.

The arrangement of the key GPS functional components described in Section 7.1, along with the key functional components of a cell-phone system is shown in Figure 8.

Figure 7: NJ2020 in a cell phone A-GPS architecture

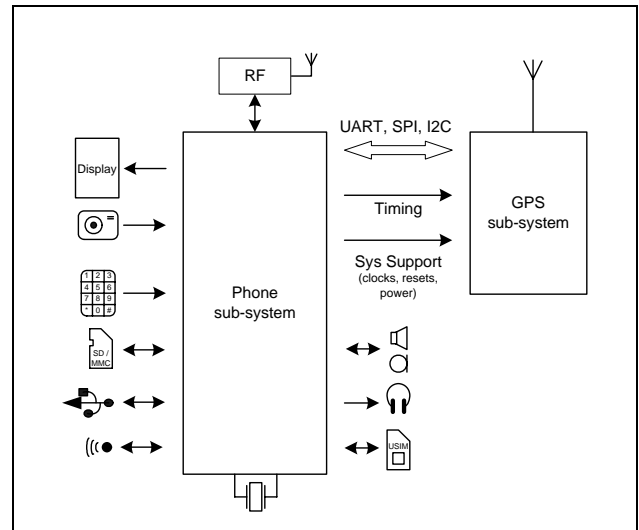
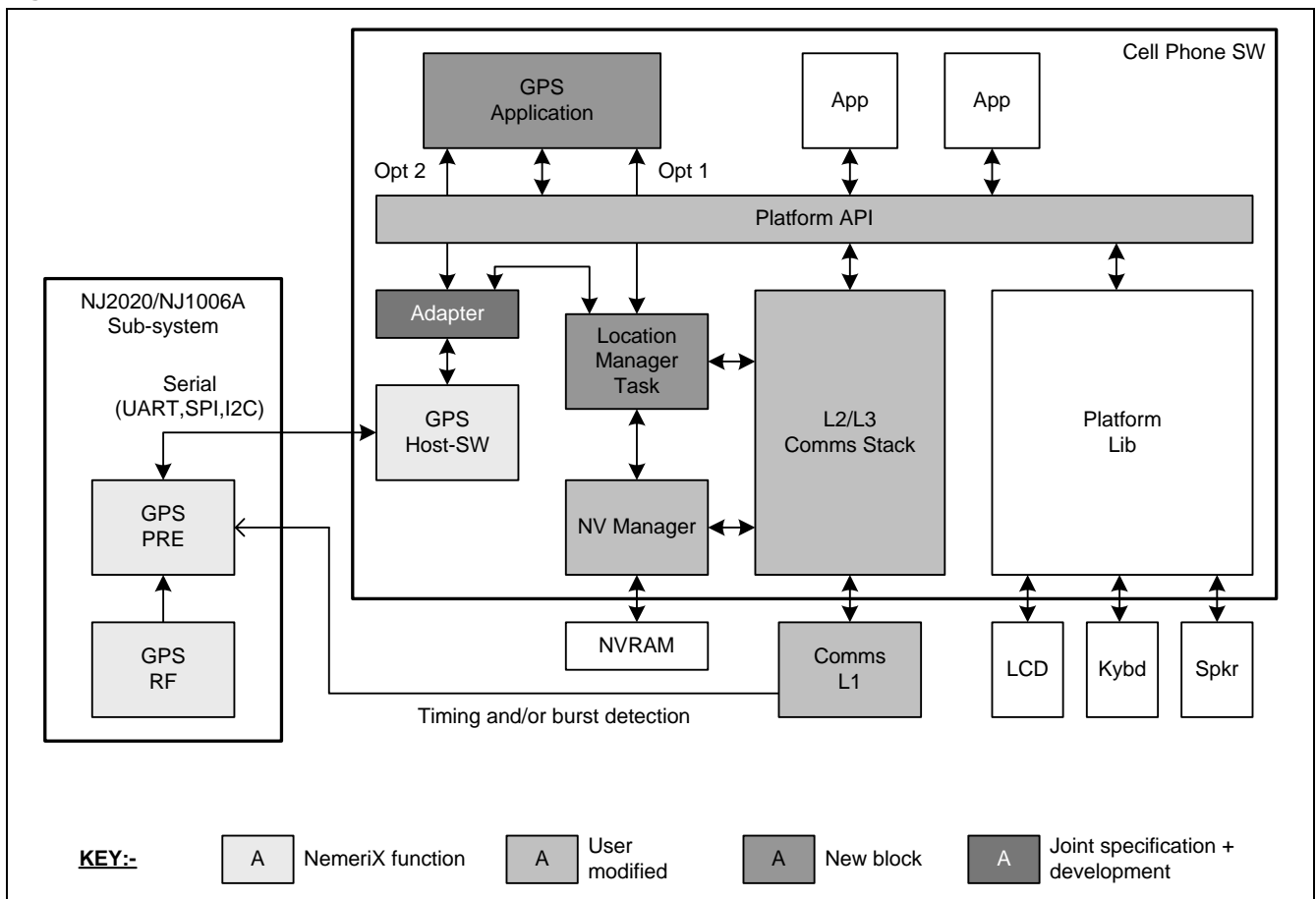


Figure 8: Software functional components in a cell phone application

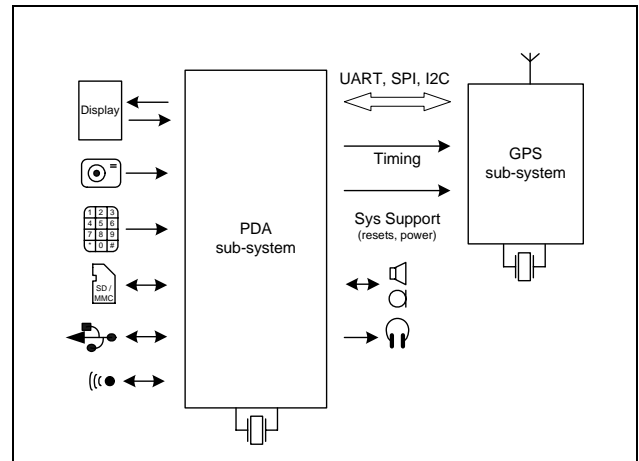


The most likely arrangement (but not the only one) is for the NAV-SW to be integrated below a 'Framework API' alongside the communication protocol stack (e.g. GSM/GPRS, WCDMA, ...). It is most likely to be contained in a wrapper or IWU (Inter-Working Unit) to translate cell-phone host messages and services into those of the NAV-SW. A GPS application will then run above the Framework API and tap into the location service interface now offered by the Framework API.

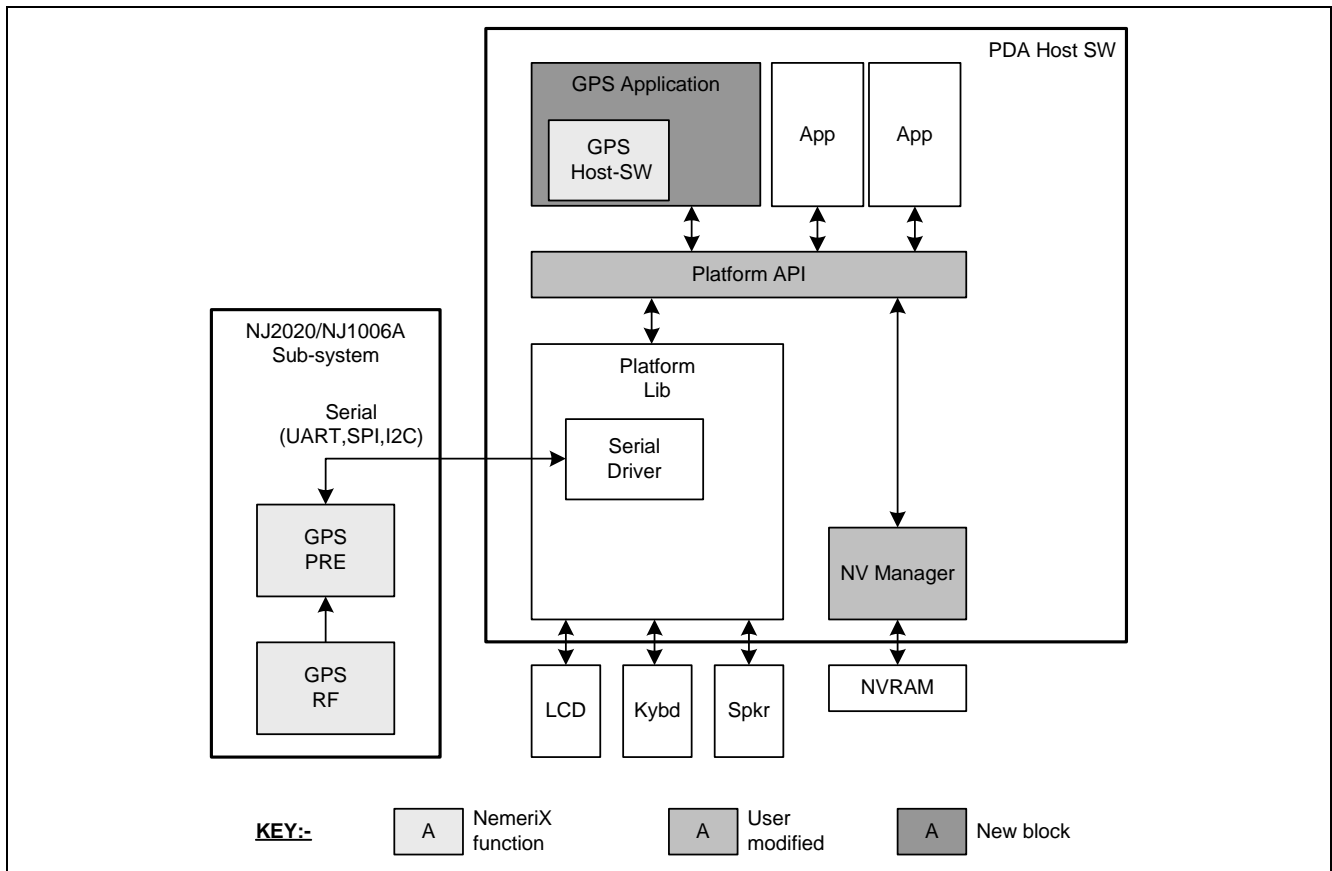
**11.2 PDA Host**

Figure 9 represents the use of the NJ2020 device within a PDA host system. A UART/SPI/I2C communication channel and other system support signals (such as Power and Resets) are all that are required. This integration model is also relevant for embedding the NJ2020 within dedicated GPS equipment provided there is a separate processor for the user interface and general control.

**Figure 9: NJ2020 in a PDA hardware architecture**



**Figure 10: Software functional partitioning in a PDA system**



The arrangement of the key GPS functional components described in section 7.1, along with the key functional components of a PDA system is shown in Figure 10. Here the most likely arrangement is for the NAV-SW to be integrated into a GPS application that sits above the Platform and Framework API. A serial API is used by the

NAV-SW to access the serial port via a device driver while the rest of the GPS application uses the other functions available from the Framework (eg. Graphics functions). Assistance data is unlikely to be available in this application, but the system NVRAM functions can be used to store almanac and ephemeris data.

## 12 Packaging

The NJ2020 will be available in 6x6mm, 0.5mm pitch, 81 pins,  $\mu$ BGA package.

## 13 PCB Layout Recommendations

The best performance is generally achieved when the NJ2020 is placed over a solid ground plane with as little interruptions as possible.

In a multilayer PCB internal layers can be used as ground plane instead of the bottom layer. It is however recommended to leave some spacing (at least 0.3mm) between the top layer and the ground plane, as this reduces losses and stray capacitances. Using layer 2 as ground plane with layer 1 for the routing is not recommended, as this results in too little spacing for most PCB build-ups.

Standard PCB materials such as FR4 can be used. Special low-loss substrates are in most cases not required to achieve proper performance, and would give only moderate performance improvements.

In order to avoid interference to the receiver from digital switching noise all digital signals shall be routed away from sensitive analog connections while some shielding is recommended. Most sensitive are the antenna and the LNA, followed by IF filter. Application note AN-002 gives several recommendations on how to prevent interference and should be read before starting a PCB design.

Operation of the analog portion of the GPS baseband processor (oscillators, AD converter inputs) could also be disturbed by an improper PCB design. In order to get good performance from the NJ2020 the following recommendations should be followed.

- Proper connections are important if good performance is to be achieved. The RF connections to the antenna and SAW filter shall be made with 50 $\Omega$  striplines (unless their length does not exceed a couple mm), while vias on all RF connections shall be avoided.
- Decoupling capacitors shall be connected very close to the chip using traces as wide as possible, with the other side of the capacitor well grounded (2-3 vias).
- Ground/power planes shall be used. All VSS supplies shall be connected to the ground plane with short lines (fan-outs and vias) and the ground plane shall be kept continuous and with as little interruptions as possible, in order to minimize stray inductance.
- All DVDD, LVDD\_XX pins shall be connected to a power plane, possibly placed just above or below the layer chosen as ground plane.
- The spacing between power and ground planes should be minimized by minimizing the thickness of the dielectric between them. This reduces leakage inductance between power and ground planes and

thus radiated EMI. A good choice could be to use two layers separated by a single layer of prepreg as ground and power planes.

- The tracks connecting the TCXO or the ATR crystal to the NJ2020 are sensitive to crosstalk from digital signals. Please keep these connections as short as possible, mount the ATR crystal and its load capacitors close to the NJ2020 package and do not cross TCXO or ATR tracks with digital tracks. An ATR going too fast is in most cases the result of interference to the ATR crystal.
- A very effective means to reduce radiated EMI is to keep all tracks carrying digital signals as short as possible and their capacitive load – including strays - as small as possible. Stray capacitances may be reduced by increasing the spacing from the routing to the ground/power planes, e.g. by placing a thicker PCB core between them. This is obviously particularly important in modules with integrated antenna.

To guarantee proper mounting of the IC, it is recommended that the PCB land pattern shown in Figure 11 is used. In particular the following requirements shall be adhered to:

- The PCB shall meet the solderability requirements of IPC/JEDEC J-STD-003A and shall be flat to within 0.1mm per cm.
- All BGA lands shall be connected with traces of similar size, such that they have a similar thermal mass. Ground/power planes shall not be connected directly to a land - a thermal trap (via, fan-out) is required. This is to improve soldering and to reduce the chance of cold solder joints.
- Vias inside PCB lands shall be plugged and metallized on top to prevent solder from wicking through the via hole. Unplugged vias inside PCB lands are not allowed.
- A solder mask with tight openings is recommended to ensure that some solder mask remains between the PCB lands.
- Any unrelated copper under the package (traces, fan-outs) shall be completely covered with solder mask. Via holes shall also be covered, no solder mask opening is allowed. This is to prevent that short-circuits between adjacent balls may occur.

PCB layout examples can be found in the NB2040 datasheet. PCB Gerber of data of such device is also available and can be used as recommended layout.

## 14 Mounting Recommendations

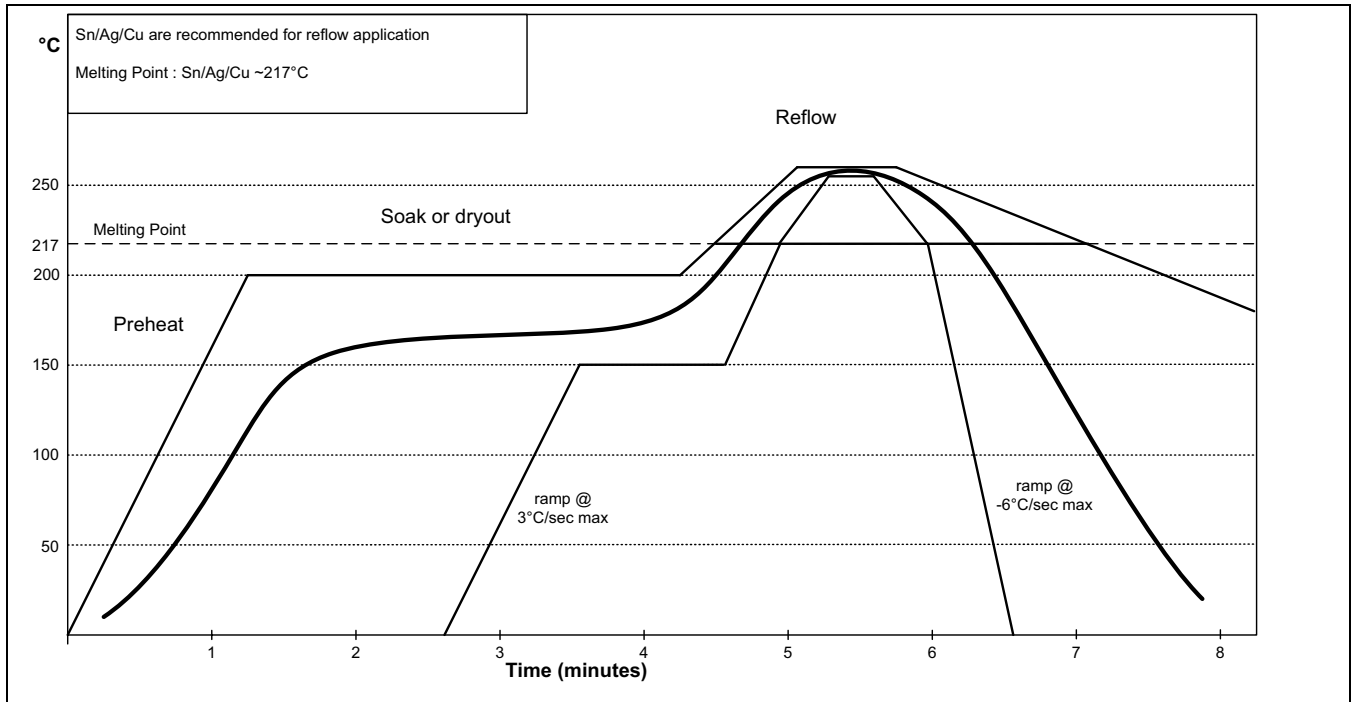
The NJ2020 shall be mounted on the PCB by reflow soldering. Please follow these recommendations:

- Stainless steel stencils with a thickness of 125-150 $\mu$ m are recommended for solder paste application. For improved solder paste release the walls of the apertures should be tapered.
- Pb-free solder paste shall be used. Sn/Ag/Cu alloys with a melting point of 217°C are recommended. A typical reflow temperature profile is shown in Figure 11. The recommendations given by the solder paste manufacturer should also be followed.
- Typically, the area under the profile curve, bounded by the liquids temperature, defines the quality of the solder joint. Too little area leads to cold solder joints, which are a reliability risk. Too much area could result in undesirable metallurgical issues that could also be a reliability risk.
- Mounting the NJ2020 with Pb-containing alloys such as the old Sn60%-Pb40% alloy is possible but is not recommended and deprecated. The user will need to run appropriate experiments to define reflow conditions and possible reliability issues if alloys other than Sn/Ag/Cu are desired.
- After assembly the board shall be cleaned to remove solder flux residue. Solder flux residue between pads or on RF components may cause high leakages which may increase RF losses to an unacceptable level. Ultrasonic cleaning shall not be used since many parts - especially crystals, SAW filters and TCXO - may be damaged. No-clean solder flux may be used to minimize cleaning requirements.

**Table 4: Classification reflow profile**

Profile Feature	Pb-Free Assembly
Average Ramp Up Rate	3 °C/second max.
Preheat Temperature Min ( $T_{Smin}$ )	150 °C
Temperature Min ( $T_{Smax}$ )	200 °C
Time ( $t_{Smin}$ to $t_{Smax}$ )	60 to 180 s
Time maintained above $T_L$ $t_L$	217 °C 60 to 150 s
Peak/Classification Temperature ( $T_P$ )	260 °C
Time within 5 °C of actual Peak Temperature $T_P$	20 to 40 s
Ramp-Down Rate	6 °C/second max.
Time 25°C to Peak Temperature	8 minutes max.

**Figure 11: Recommended reflow profile for lead-free solder paste**



### 15 Physical Dimensions

Figure 12: BGA 6mm x 6mm, 0.5mm pitch package specifications

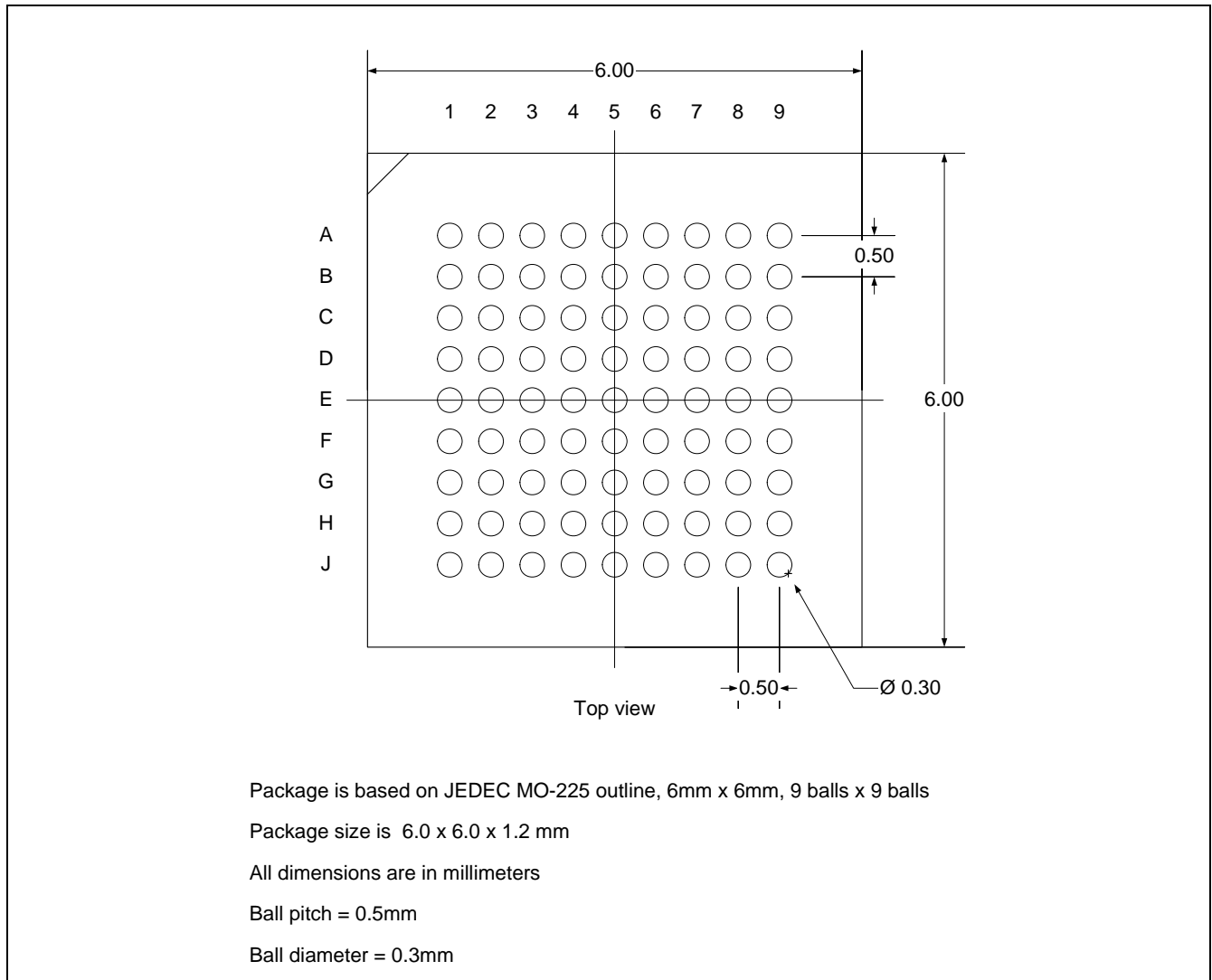
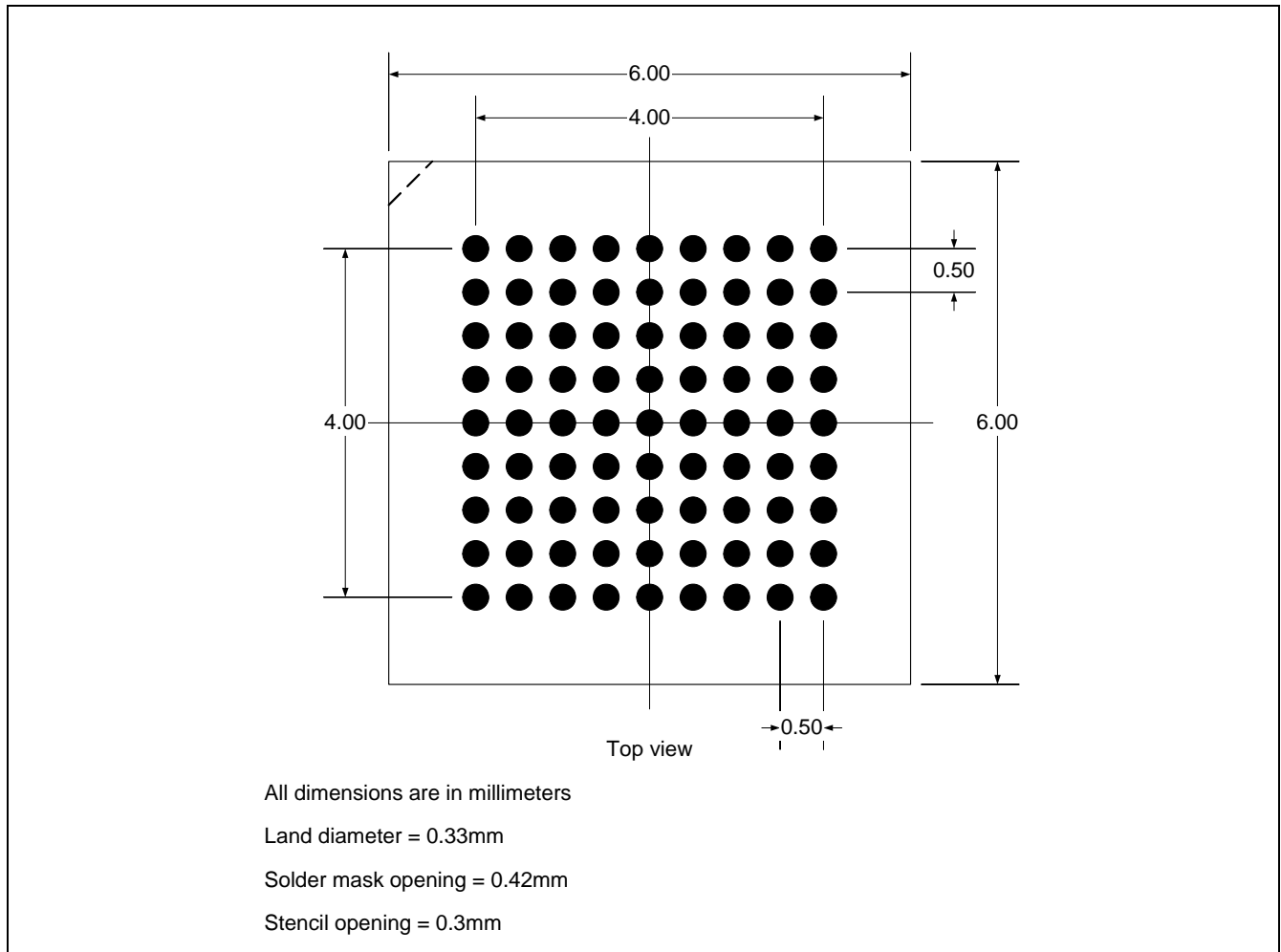


Figure 13 : NJ2020 - 6x6mm, 0.5mm package footprint



**Notes:**

**Ordering information**

Part	Description
NJ2020	GPS Baseband Processor

**Related products**

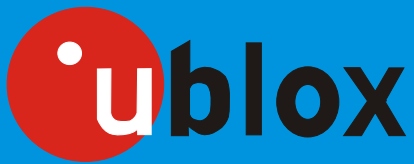
Part	Description
NJ1006A	GPS RF Front-End
NS2020	A-GPS SW Platform
NB2040	Reference Design
EK2040	Evaluation Kit

Nemerix SA  
Headquarters  
Stabile Gerre 2000  
PO Box 425  
6928 Manno  
Switzerland

Phone +41 91 612 4700  
Fax +41 91 612 4701  
email sales@nemerix.com

**LEGAL NOTICE:**

NEMERIX PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR IN APPLICATIONS WHICH INVOLVE POTENTIAL RISK OF DEATH, PERSONAL INJURY OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE IN CASE OF FAILURE OR MALFUNCTION OF THE PRODUCT.



瑞士u-blox公司 全线产品代理

联系方式:



洪 维

King Hong

市场部

15012591515

飞扬科技(香港)有限公司

深圳市蝴蝶谷科技有限公司

Shenzhen Rise Technology co., LTD

地址: 深圳市福田区车公庙工业区201栋东座7楼

电话: 0755-81306214 传真: 0755-83318188

E-mail: GPSbaby@gmail.com http://www.GPSbaby.com

主要产品线:



U-blox 全系列GPS模块

U-blox GPS原装板卡/评估套件

U-blox GPRS模块



RISE-GPS系列u-blox GPS模块评估板  
专业化成品GPS板卡



RISE-M系列GPS模块  
大客户订制GPS解决方案



RISE 800MHz高速ARM11嵌入式CPU  
支持DDR2代内存及H.264硬解压和2D及3D图形加速



MID及UMPC方案  
PCBA方式及专业产品大客户订制模式



GPS电子罗盘成品  
GPS导航仪, GPS电子警示器