

**Features**

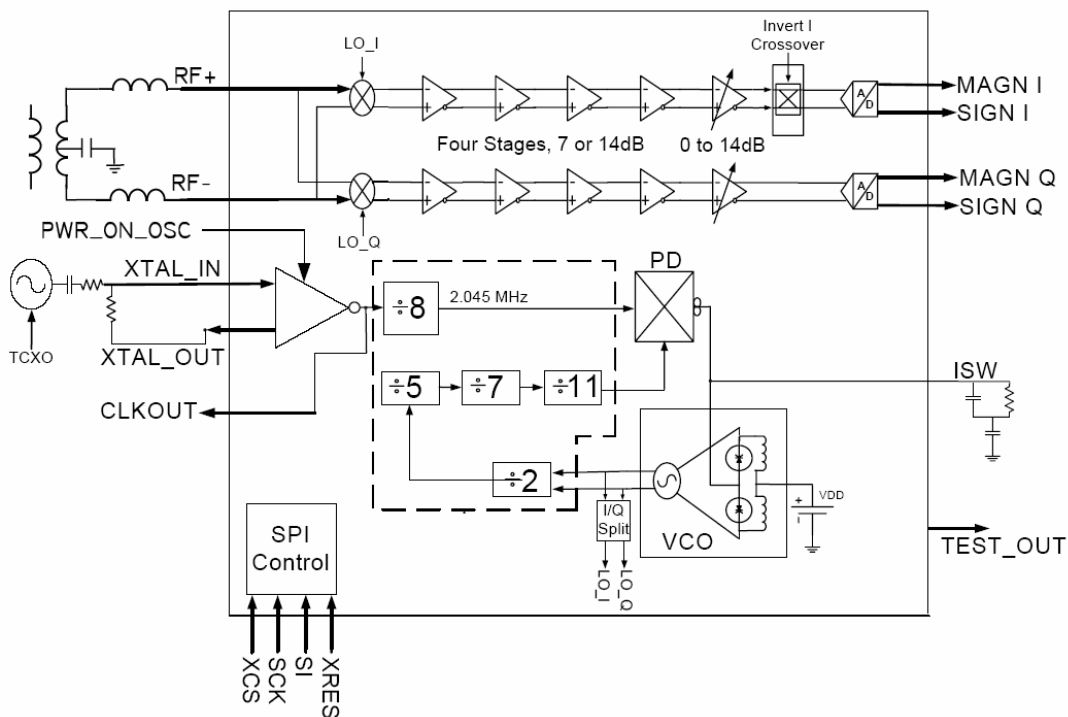
- Single-chip RF front-end for a GPS receiver
- Intended for 50  $\Omega$  systems
- Adjustable gain
- Low-power modes
- User-controllable through SPI serial interface
- 16.3676 MHz reference clock input, both crystal and external oscillator are supported
- Small area QLP-20 package, 4x4x0.9mm<sup>3</sup> size
- Glue-less interface to *uN8031B* and *uN8130* GPS baseband receiver chips
- Level-shifted interface signals to *baseband*

**Description**

*uN8021C* is a single-chip GPS L1 band RF front-end to be used together with a *uN8031B* or *uN8130* GPS baseband receiver-processor chips. The *uN8021C* supercedes the *uN8021B* and contains a mixer, voltage controlled oscillator (VCO), frequency synthesizer and two analog to digital (ADC) converters. The chip can be controlled through an SPI serial interface and it is based on the direct conversion principle with on-chip filtering. It has adjustable gain and a near zero intermediate frequency (IF).

**Block Diagram**

The *uN8021C* block diagram and typical analog connections are illustrated below:



**Figure 1. uN8021C Block Diagram**

## Pin Description

The pin description for the uN8021C defined for the QLP-20 package is in table 1 below:

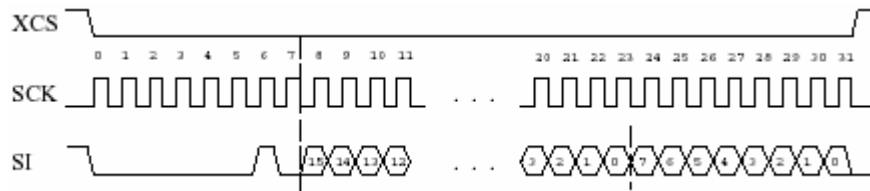
Pin #	Name	Description
1	VDD_RF_IF	Analog power for the RF I/O including XTAL_IN, XTAL_OUT, ISW, TEST_OUT, RF+, and RF- pins.
2	RF+	Positive input of differential RF-input.
3	RF-	Negative input of differential RF-input.
4	VDD_VCO	Analog power for the RF VCO block.
5	VDD_DIG	Digital power supply.
6	XTAL_IN	Crystal oscillator input pin (16.3676 MHz).
7	XTAL_OUT	Crystal oscillator output pin (16.3676 MHz).
8	TEST_OUT	I/Q arm analog output with 10 dB attenuation
9	ISW	VCO loop filter pin.
10	PWR_ON_OSC	Enable/power-down control input for the crystal oscillator. Enables the oscillator when driven high.
11	CLKOUT	Clock output (16.3676 MHz), buffered output from crystal oscillator.
12	MAGN_I	In-phase arm IF signal magnitude output.
13	SIGN_I	In-phase arm IF signal sign output.
14	MAGN_Q	Quadrature arm IF signal magnitude output.
15	SIGN_Q	Quadrature arm IF signal sign output.
16	XRES	Active low asynchronous reset input.
17	SCK	SPI serial clock input.
18	XCS	Active low chip select.
19	SI	SPI serial data input.
20	VDD_IO	Digital I/O power supply for PWR_ON_OSC, CLKOUT, I and Q, XRES, SCK, XCS, and SI pins; 3V or 1.8V.
-	GND	The ground (GND), which is common to both the digital and analog parts of the chip, is not connected to any pin. Instead, the bottom of the lead frame acts as a ground connector.

**Table 1. uN8021C Pin Description**

## Register Programming

### SPI Interface

The *uN8021C* is controlled through an SPI interface. The interface contains data input only (SI pin), so the control registers can not be read. The data width (and thus the register width) is 8 bits, while the address is 16 bits. The timing of SPI interface is as follows:



**Figure 2. SPI Timing Diagram**

In the *uN8021C*, there is a total of three registers, occupying addresses 0x00 to 0x02. These registers are as follows:

Address	Name	Description
0x00	IGAIN	I-channel gain settings
0x01	QGAIN	Q-channel gain settings
0x02	CTRL	General RF control

**Table 2. uN8021C Programmable Registers**

### IGAIN and QGAIN Registers

The gain control registers IGAIN and QGAIN contain the same control bits, but IGAIN controls the I-channel gain while QGAIN controls the Q-channel. The bits of these registers are defined as follows:

Bit	Description
7	Reserved, program to 0
6	+7dB gain for the first amplifier
5	+7dB gain for the second amplifier
4	+7dB gain for the third amplifier
3	+7dB gain for the fourth amplifier
2	Bit 2 of ADC gain setting
1	Bit 1 of ADC gain setting
0	Bit 0 of ADC gain setting

**Table 3. IGAIN and QGAIN Register Definition**

The ADC gain setting (three bits with bit 2 most significant and left-most) has the following possible values:

ADC setting	Description
000	+0 dB
001	+2 dB
010	+4 dB
011	+6 dB
100	+8 dB
101	+10 dB
110	+12 dB
111	+ 14 dB

**Table 4. ADC Gain Setting Definition**

The maximum gain of +42dB is achieved by setting all bits of the gain register high. This programmable gain is added to the base gain of 43 dB. When adjusting the gain values, the best noise performance is achieved by using as high gain as possible in the first amplifier stages (control bits 6 and 5). After reset, IGAIN and QGAIN registers contain the hexadecimal value 00.

### CTRL Register

The general RF control register CTRL contains the following control bits:

Bit	Description
7	Enable I-channel test, program as 0
6	Enable Q-channel test, program as 0
5	Program as 0
4	Invert sign bit of I-channel output, effectively swaps the I- and Q-channel. Program as 0.
3	Disable frequency synthesizer clock
2	Power off VCO
1	Power off frequency synthesizer
0	Power off IF and RF

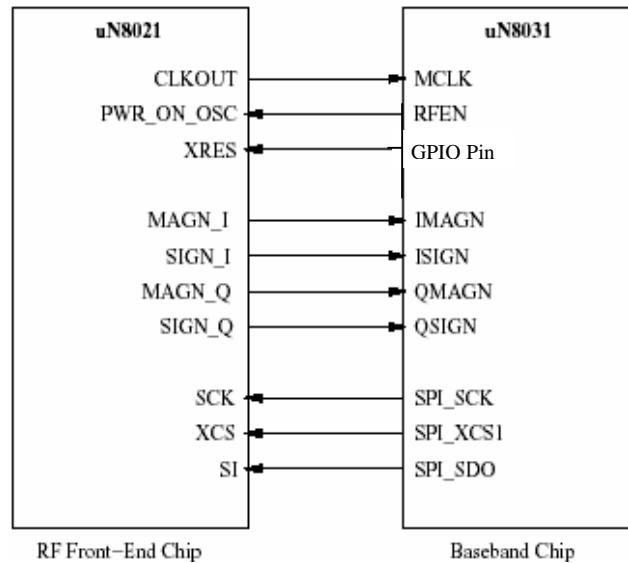
**Table 5. CTRL Register Definition**

The bits 4,5,6 and 7 are used for testing only, and should always be set to zero by the user. After reset CTRL contains the value hexadecimal 00. The chip will therefore be completely powered on.

### Interconnection with baseband

The *uN8021C* external GPS RF front-end chip can be connected to *uN8031B* or *uN8130* GPS baseband processing chip using 10 signals as shown in figure 3. No external glue logic or pull-up/pull-down resistors are required. The signals can be divided into three separate function groups as follows:

- System signals (clock, reset, RF enable)
- Data signals from RF to baseband (I/Q sign and magnitude)
- Control signals from baseband to RF (SPI interface)



**Figure 3. Interconnection Diagram**

The digital interface is 1.8V or 3V CMOS logic level compliant as determined by VDD\_IO. All I/O pins must be the same levels, mixed 3V and 1.8V I/O is not supported.

## Electrical Characteristics

### Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit
Storage temperature range	$T_{STG}$	-55	+150	°C
Operating temperature (ambient)	$T_A$	-40	+85	°C
Maximum power dissipation ( $T_A = +85\text{ °C}$ )	$P_D$		500	mW
Peak Reflow Temperature	$T_{PEAK}$		215	°C
Current on any pin to avoid latch-up	$I_{MAX}$	-30	+30	mA
ESD protection	$V_{ESD}$	1000		V
Supply voltage, analog VDD_RF_IF and VDD_VCO	AVDD	-0.3	3.6	V
Supply voltage, digital VDD_DIG	DVDD	-0.3	3.6	V
Supply voltage, digital I/O VDD_IO	IOVDD	-0.3	3.6	V
Input pin voltage, I/O	$V_{IO}$	-0.3	IOVDD+0.3	V
Input pin voltage, analog	$V_{ANA}$	-0.3	IOVDD+0.3	V

**Table 6. Absolute Maximum Ratings**

Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### Recommended Operating Conditions

Item	Symbol	Min	Typical	Max	Unit
Operating temperature	$T_A$	-40		+85	°C
Supply voltage, analog , analog VDD_RF_IF and VDD_VCO	AVDD	2.7	3.0	3.3	V
Supply voltage, digital VDD_DIG	DVDD	2.7	3.0	3.3	V
Supply voltage, digital I/O VDD_IO in 1.8 and 3V ranges	IOVDD	2.7 1.7	3.0 1.8	3.3 1.9	V

**Table 7. Operating Temperature and Voltage Range**

AVDD and DVDD should be at the same voltage level; however, IOVDD may be at a different voltage level. VDD\_IO features both 1.8V and 3.0V nominal ranges. Operation of the product at -40C is assured with ATE guard banded conditions at room temperature test point. Updates are done to these limits as needed and in accordance with the u-Nav policy of change notification.

### Digital Signal Characteristics

Item	Symbol	Test Condition	Min	Max	Unit
Input high voltage	$V_{IH}$		0.7xIOVDD	IOVDD+0.3	V
Input low voltage	$V_{IL}$		-0.3	0.3xIOVDD	V
Output high voltage	$V_{OH}$	$I_{OH} = 1\text{mA}$	0.7xIOVDD	IOVDD	V
Output low voltage	$V_{OL}$	$I_{OL} = -1\text{mA}$	0	0.22xIOVDD	V
Input leakage current, at 25 °C	$I_{LI}$		-1.0	+1.0	μA

**Table 8. Digital DC Characteristics**

Item	Symbol	Min	Typical	Max	Unit
RF oscillator clock cycle	$t_{OSC}$		61 <sup>note 1</sup>		ns
RF oscillator setup time in clock cycles	$t_{STABIL}$		4096		Clocks
VCO setup time	$t_{VCOstart}$		15	30	mS
Clock cycle, CLKOUT	$t_C$		61 <sup>note 1</sup>		ns
Clock duty cycle, CLKOUT	$t_{DUTY}$	45		55	%
SPI Clock	$F_{SPI}$			5	MHZ
Digital input pin capacitance	$C_i$			3	pF
Digital output load capacitance	$C_L$			20	pF

**Table 9. Digital AC Characteristics**

<sup>1</sup> Note that the RF oscillator frequency should be 16.3676 MHz for normal operation with the baseband, so the 61 ns clock cycle is not exact.

### Operating Power Consumption

The power consumption represented in the table below is at nominal condition of DVDD=3.0v, 25°C.

Item	Description	Min	Typical	Max	Unit
Active Mode	State after XRES assertion with PWR_ON_OSC=1, all functions on with CTRL bits 3..0 set to 0	45	62	79	mW
Sleep, clock enabled	All functions disabled, PWR_ON_OSC=1 with CTRL bits 3..0 set to 1	0.0	6	15	mW
Sleep, clock disabled	All functions disabled, PWR_ON_OSC=0 with CTRL bits 3..0 set to 1	0.0	0.03	0.09	mW

**Table 10. Operating Power Consumption**

### Analog Signal Characteristics

Item	Symbol	Min	Typical	Max	Unit
XTAL IN input impedance	$Z_{XTI}$		1		MΩ
I/Q gain imbalance	$G_{IQ}$		0.5	1.5	dB
Phase noise <sup>note 2</sup>	NP		-67	-60	dBc
I/Q Magnitude Bit Threshold <sup>note 3</sup>			-38		dBm
Noise figure <sup>note 4</sup>	NF		20		dB
1dB compression at input <sup>note 5</sup>	$P_{1dB}$	-43	-40		dBm
-3dB Bandwidth	BW	3	4	5	MHz
XTAL IN input level	$V_{XTI}$	0.5	0.8	DVDD	V <sub>pp</sub>

**Table 11. Analog Signal Characteristics**

<sup>2</sup> Phase noise measurement is calculated as the difference in the signal level from the IF image reference point to a point 10KHz offset from the image. The measurement was taken with the I/Q Gain setting of 67hex value.

<sup>3</sup> The I/Q Magnitude Bit Threshold is represented as the minimum RF input level required to make the I/Q MAGN Bits first start toggling at the minimum gain setting.

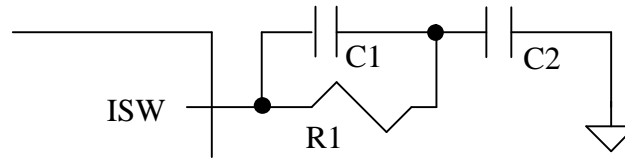
<sup>4</sup> The Noise Figure was measured with I/Q Gain setting of 67hex value.

<sup>5</sup> Compression point was measured with gain register at 0dB setting.

## Applications Information

### *PLL Loop Filter*

Though the loop filter can be implemented in a variety of ways, the recommended uN8021C VCO loop filter topology and component values are listed below:

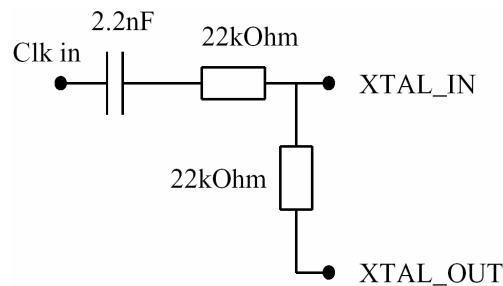


**Figure 4. Recommend Loop Filter**

Item	Typical	Unit
R1	15K	ohm
C1	33	pF
C2	1000	pF

### *TCXO Coupling Network*

When using an external reference clock, the circuit below is recommended to attenuate and DC isolate the source. The voltage input to the coupling network of figure 5 should exceed minimum  $V_{XTI}$  volts. Note that in this configuration, XTAL\_IN is a virtual summing junction due to feedback from XTAL\_OUT.



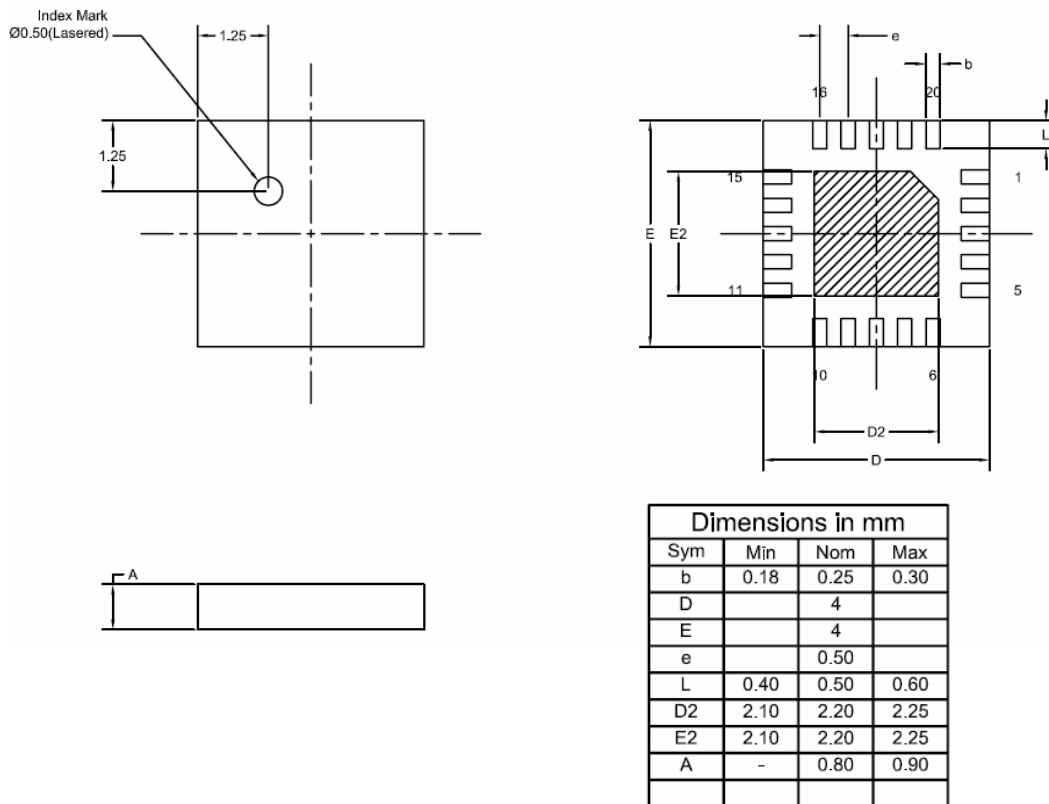
**Figure 5. External Reference Clock Coupling**

### *Wake-up and MCLK Delay*

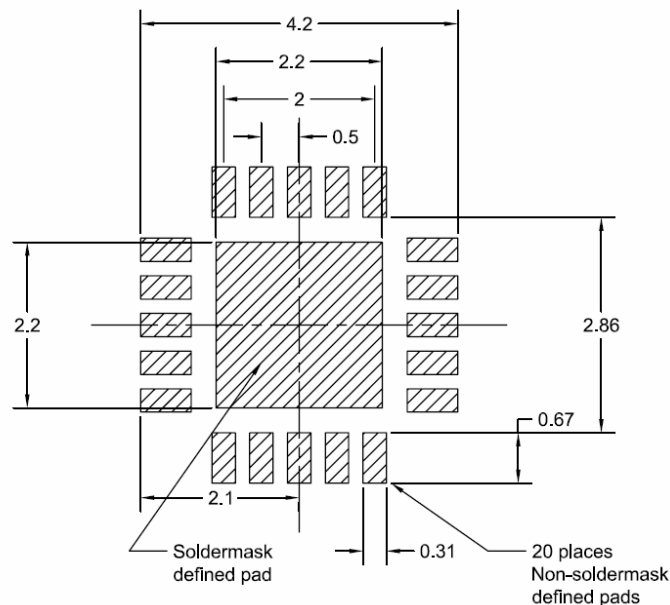
When using the uN8021C with the uN8031 baseband and waking up from sleep, designs powering on a TCXO with PWR\_ON\_OSC assertion are subject to a valid CLKOUT race condition. This occurs during the TCXO start-up period (typically 500 to 1000uS in duration) because transients amplified in the RFIC clock buffer toggle CLKOUT erratically. Though the uN8031 provides clock conditioning of 4096 transitions, under some conditions this may not be enough. Placing a resistor/capacitor network to delay PWR\_ON\_OSC assertion at the RFIC during TCXO startup provides a solution. Typically, 100K series resistance from baseband RFEN to PWR\_ON\_OSC and a 10nF capacitor from PWR\_ON\_OSC to ground is sufficient for most TCXOs. These steps are not required when using the uN8130 baseband.

### Package Description

The uN8021C is packaged into a QLP-20 package. The package dimensions (in millimeters) and pin numbers are shown below in figure 5.



**Figure 4. uN8021C Package Physical Dimensions**



**Figure 5. uN8021C Recommended PCB Package Footprint**

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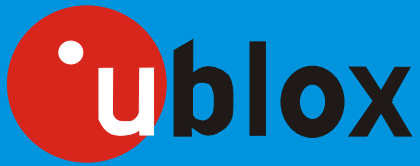
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PCBA方式及专业产品大客户订制模式



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